AVP254

FAQ - Frequently Asked Questions

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Access to the Product Web Page

Access to the Product Sheet

Summary

Introduction

This document is a **FAQ** (**F**requently **A**sked **Q**uestions) document about Oxytronic AVP254.

AVP254 is an Automatic Verification Platform for FPGA verification in Safety-Critical Applications. It enables FPGA virtual simulation together with On-Board testing on the final destination board.

1. General Questions

1.1. Can I use AVP254 for non-avionics projects (no DO-254)?

Yes.
AVP254 has been designed by Oxytronic, originally for our own projects, following the DO-254 guidelines for Aeronautics. But our solution is not locked at all to the DO-254, not even to any standard.

It should be used in the following conditions:

1. You need to verify your FPGA on the final destination board (meaning, neither the FPGA alone, nor the FPGA on an intermediate board which is not the final application board)
2. Your development flow is Requirements-Based
3. Workload for the physical verification of your FPGA is high

That means AVP254 is relevant for Safety-Critical FPGA in various domains like:

- ISO-26262 (Automotive)
- IEC 61508 and its derivatives (Industrial, Railways, Healthcare)
- IEC 62566 (Nuclear power plant)
- ECSS-Q-ST-60-02 (Space)
- or other standards.

1.1. Can I use AVP254 to verify an ASIC?

Yes, as soon as source files provided are readable by a simulator, like ModelSim: VHDL or Verilog files, compiled libraries…

1.2. Can I use AVP254 to verify a board?

Yes, but only digital components like FPGA or ASIC can be simulated.

1.3. What are the main assets of AVP254?

- **Credibility towards certification authorities** :
  - Thanks to the strict virtual/physical equivalence, you can provide a test coverage ratio on the board which is the same as for virtual simulation.
  - Verification can be done in best/worst case for temperature and power voltage.
  - Real world tests including clock shifts and all hardware deviations
- **Time saving** :
  - You do not have to spend any time to develop and implement a testbench for your application; the test setup for both physical and simulation verification already exists.

- Fully automatic and auto checking solution: Launch all the test patterns with on mouse click, wait and get the verification status: OK or KO.
- You write a unique set of test procedures and you choose to execute them either on the virtual simulator, or on the target board.
- Non-regression tests can be executed directly on the physical bench. Important gains can be observed.
- Long period events (ie more than 10 seconds) can be tested at real time speed instead of waiting for endless simulations.

- **Return On Investment** :
  - Our solution is based on the PXI standard which is widely spread in industry, and most of the hardware can be reused without any investment from applications to applications.
  - Our solution uses as inputs and outputs text and/or Word documents that can be generated and post-processed by your existing tools.
  - Use your existing virtual simulator.
  - Easy migration of the testbench to production tests.
- **Technical assets** :
  - Our solution can handle bi-directional signals.
  - Physical verification and virtual simulation can be executed independently (it is not required to get simulation results for the physical verification execution).
  - Our solution can use algorithms models for verifications from most of the industry standard modeling tools (Matlab, Labview, C#, …)
  - Issues founds during hardware physical tests can be reproduced in simulation to watch device internal signal for easy debug.
  - Logs files contain not only auto check OK or KO status but also detailed measurement performed by AVP254 for deeper analysis or device characterization.

1.4. What are the product limitations?

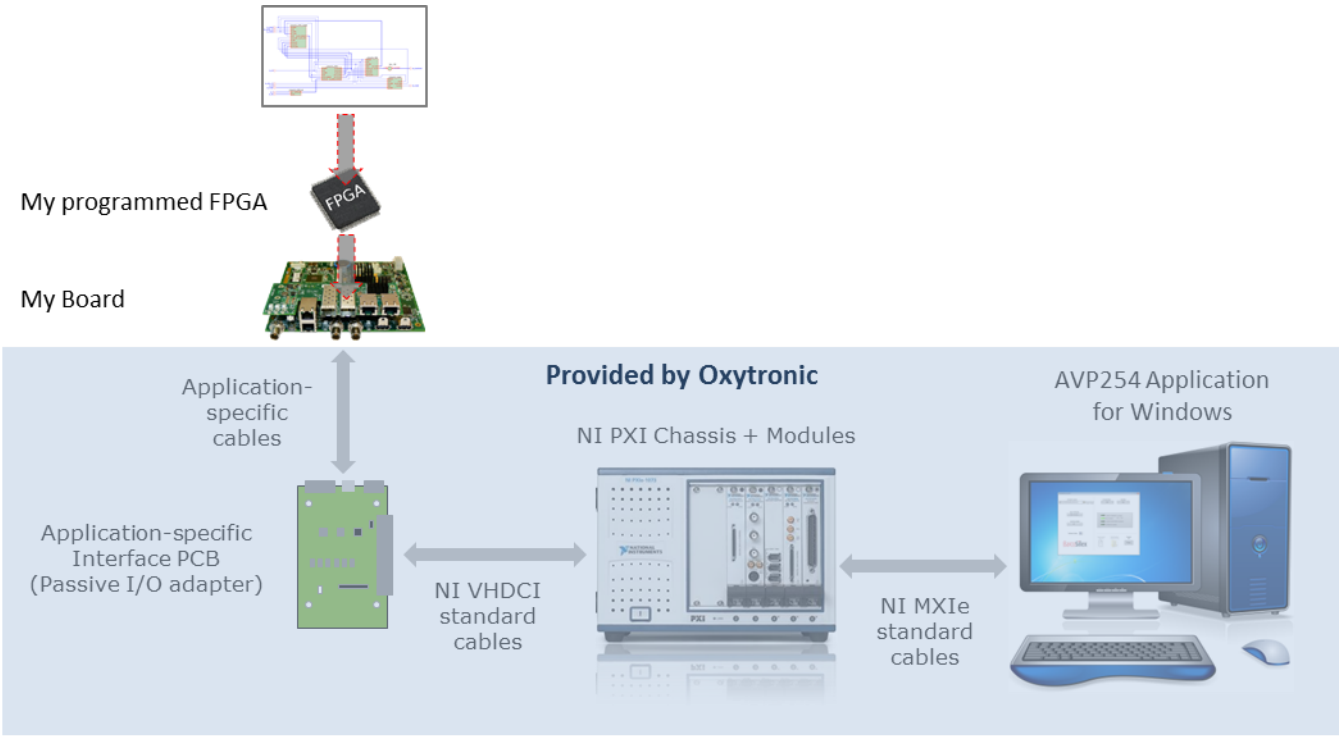
Application is limited to the maximum frequency of the PXI hardware (i.e. sampling freq = 200 MHz).

1.5. Which virtual simulation tools are compatible?

- Mentor Graphics Modelsim
- Other tools on demand

1.6. Considering all elements of the solution, what is provided by Oxytronic?

Following figure shows what we typically provide for the hardware part. Special clients requirements can also be taken into consideration (please contact us).



Our offering includes:

- The full PXI testbench with associated calibration reports, documentation and software including : test sequencer, auto-verification engine, report generation engine and GUI,
- The testbench simulation model,
- A DO-254 qualification report for all native functions,
- A testing PC,
- The design of the specific hardware interface board,
- A training for methodology understanding and platform handling,
- Additional services for the development of your verification functions: custom interfaces development and integration, DO-254 qualification report for all custom functions with associated reviews.

1.7. How to get a quotation from Oxytronic?

In order to define the HW configuration, we need customer's board and FPGA specification (at least the main architecture and I/O characteristics). Then we choose the relevant PXI chassis and modules together with the Interface PCB and cables specifications, and we evaluate time to develop custom functions and qualification report, if any. Then we can send the quotation.

1.8. Can I integrate AVP254 within a larger testing solution, including power management, external instruments management…?

AVP54 has been built upon widely spread test & measurement solutions: NI PXI and LabVIEW. Those solutions are made for easing integration in T&M applications. Specific customer needs can be discussed with Oxytronic.

1.9. Can I use AVP254 to verify a FPGA on its board, both already designed?

Yes. Even if Oxytronic will be pleased to work with you before you design the FPGA and the board in order to ease the AVP254 configuration and cut the verification costs.

2. Technical Questions

2.1. Is it mandatory to launch virtual simulation before physical verification?

No. It is an asset for AVP254. In some cases, virtual simulation to verify requirements can be very long. AVP254 enables going directly to physical verification, thanks to its strict virtual/physical equivalence.

2.2. All my FPGA I/Os are not available out of the board through a connector : how to proceed?

- Case 1 :FPGA IOs are accessible through another active component - such as a CPU - on a connector

  In this case the active component is configured to be used as an extension of the testbench. Then AVP254 accesses the FPGA IOs using this active component. For the simulation aspect, a model of the behavior of this active component is made.

- Case 2 :FPGA IOs are not accessible through another active component on a connector

  In this case Oxytronic can propose to use a bed-of-nails like PCB interface between My board and AVP254.

2.3. My board communicates with its embedded equipment using a communication protocol: how to implement this with AVP254?

AVP254 is a modular platform. A communication protocol can be implemented:

- By using a Oxytronic COTS HDL IP (already available : UART, SPI, I2C)
- By using your own specific HDL communication module within AVP254
- By asking Oxytronic to develop a specific communication module

Oxytronic will provide AVP254 with the required communication module.

2.4. My FPGA communicates on the board with other digital components (DDR, DSP…): how to proceed?

See §2.2

2.5. What kind of debugging solutions are possible with AVP254?

Debugging solutions provided by AVP254 are:

- Analysis of the measurements/checks done and reported in the detailed log files
- Chronogram analysis for all the acquired signals
- Chronogram analysis for all FPGA internal/external signals (only in simulation mode)

2.6. What does "code coverage ratio" mean exactly in AVP254?

Code coverage ratio refers to code coverage provided by the simulation tool and required by EASA certification memo EASA CM-SWCEH-001 (ie Decision, Statement and Transition coverage for DAL A Devices).
AVP254 uses the same pattern for both physical and simulation tests so that the code coverage ratio can be used to quantify the physical verification too.

2.7. How Clock Domain Crossings are addressed by AVP254?

If the FPGA under test uses several clock domains, the physical test using AVP254 will allow highlighting clock synchronization problems because it runs on the final application hardware and in real conditions (oscillators shift, temperature, voltage variations).

AVP254 can give confidence in clock domain crossing management; however AVP254 won't perform an **exhaustive** analysis of the FPGA clock domain crossing.

Oxytronic highly recommends managing clock domain crossing this way:

1- Identify all the clock domain crossing in your design (can be done by a tool)
2- Then ensure – for each clock domain crossing – that the associated resynchronization strategy matches your coding standard **and** FPGA design state of the art by a HDL code analysis

For any advice / recommendation about Clock Domain Crossing management, contact Oxytronic.